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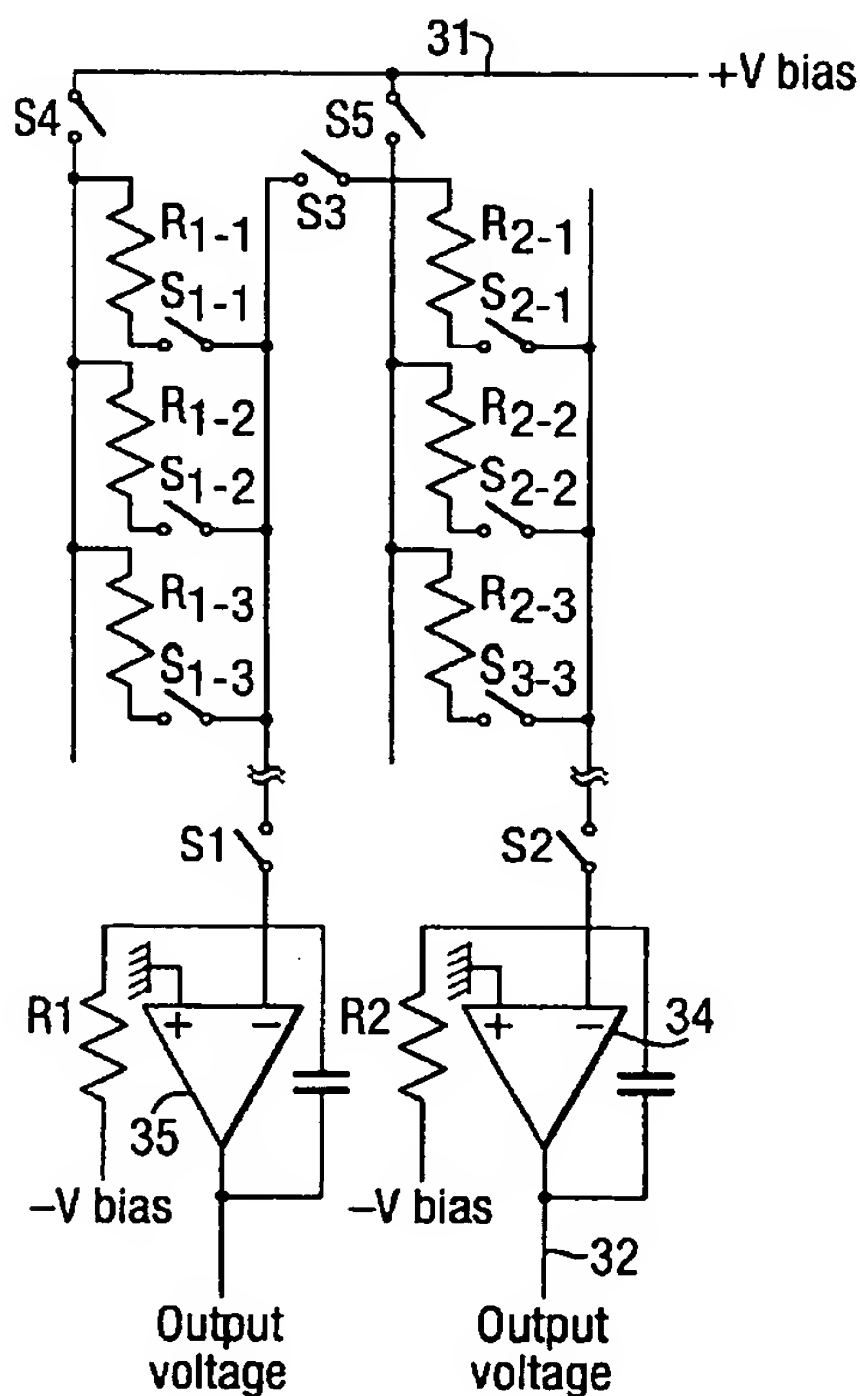
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[Continued on next page]

(54) Title: **RECONFIGURABLE DETECTOR ARRAY**



(57) Abstract: An array of detectors can be configured to be read as separate detectors, or to be connected into larger groups, e.g. groups of four (a 2x2 array). This allows the formation of a relatively high definition image, and a much faster formation of a lower resolution image. This may be used within an automobile to control deployment of safety airbags in accordance with a drivers position relative to the airbags. Preferably the array is a 64x64 array of thermal detectors.

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Declaration under Rule 4.17:

— of inventorship (Rule 4.17(iv)) for US only

Reconfigurable detector array.

This invention relates to a reconfigurable detector array, specifically but not exclusively an x, y array of thermal detectors each detector forming a pixel.

5

Such an array is usefully arranged in the focal plane of an imaging system to provide a thermal image of a scene of interest, e.g. the monitoring of rooms, paths or parking areas. Thermal imagers are useful because they can use natural radiation without addition illumination; this is particularly useful at night. Thermal imaging normally
10 operates in the radiation bands between 3-14 μ m. Other infra red wavelengths, and visible wavelengths arrays may be used by the present invention.

Some applications of infrared imaging can call for changes in frame rate or sensitivity in real time. An example of this is in the detection of head position for the correct
15 deployment of vehicle airbags in an accident. In the time leading up to the accident, it is important to locate the head of the occupant in three dimensions and, during the accident, it is important to track the motion of the head. The acquisition task can be a relatively slow one, but may require a high sensitivity to ensure that the boundaries of the head are properly acquired. Conversely, during the accident, the position of the
20 head must be tracked fast to ensure that the correct air bag is fired at the correct time.

Current thermal imagers usually have fixed readout rates and numbers of pixels. Averaging of succeeding frames of data is a common method of improving the signal-
25 to-noise ratio (in an ideal system, the ratio improves with the square root of the number of frames added). Some visible band camcorders also allow adjacent pixels to be added, trading spatial resolution for sensitivity. Random access is also possible in some devices to enable smaller sub-sets of the focal plane to be read out in a faster time. Other arrangements for connecting individual elements together are
30 described in GB-2332585A, WO-97/21080-A1, and US-5229609.

- 2 -

In currently available devices, the adding of successive frames of data and adjacent pixels is achieved in the camera processing rather than on the focal plane.

- 5 Air bag control systems currently in the market use accelerometers to control as many as six air bags to protect the occupants in an accident. The optimum timing and degree of inflation of each bag must be varied to ensure the best protection. Relying on acceleration readings alone does not take into account the position of the occupants and errors can occur. The bags may inflate too close the person, or the
- 10 bag may have deflated before the person reaches it. Failure to inflate the correct bag may also leave the person vulnerable.

- A visible imager will require a wide dynamic range to allow for both full tropical sunlight through an open sunroof and twilight. It will require an active illumination
- 15 system at night.

- A thermal imager will operate by day or by night as the human head emits radiation that it can image. However, there will be times when the apparent temperature of the interior parts of the car close to the occupant (headrest, seatback etc) are close to or
- 20 the same as the temperature of the occupant's head. In this latter case, the sensitivity of the imager may have to be increased to be certain of acquiring the head position correctly.

- The above problem is solved, according to this invention, by connecting several
- 25 separate detectors together as required and keeping each detector separate at other times.

- 3 -

According to this invention a reconfigurable detector array comprises:

a substrate carrying an x by y array of detectors each detector forming a pixel,
electrodes for receiving an electrical signal from each detector independently,
characterised by connections for connecting separate detectors to be read

- 5 individually and into larger groups as required without changing substantially the effective impedance.

Preferably the substrate carries electronic circuitry, amplifiers, switches etc, for
processing the outputs of each detector and for reconfiguring the array into e.g.

- 10 groups of four (2x2), nine (3x3), or sixteen (4x4) etc. detectors without changing the effective impedance.

The array may include optical means for directing a scene onto the detectors.

- 15 The values of at least x or y may be in the range 24 to 96 inclusive.

For an array of thermal detectors e.g. resistance bolometers, the array and substrate
with electronic circuitry is preferably encapsulated to isolate the detectors from
ambient conditions.

20

A 64x64 pixel focal plane might provide 100mK sensitivity at standard frame rate, e.g.
30Hz.

The detectors are small resistors and the readout circuit is optimised to work with a
25 given input impedance.

- 4 -

If the focal plane array is reconfigured by joining up sets of 4 detectors to make a 32x32 array, by connecting 2 detectors in parallel and two pairs of paralleled detectors in series, then the resistance of the quad of detectors remains the same as far as the readout amplifier is concerned, and the thermal time constant of the bridges remains the same as before. However, as 4 signals have been averaged, the noise reduces by the square root of 4, i.e. by 2. The sensitivity is thereby improved to 50mK. It will be appreciated that the bias power to the individual detectors must be maintained to avoid a loss in response. Conveniently this may be achieved by increasing the overall bias voltage supplied to the array.

10

Also, as the number of nodes to be read out is now only 32x32, rather than 64x64, yet the clocking rate remains the same (as the time constants have not changed), it is possible to take 4 sets of readings of the 32x32 array in the same time as it would have taken to read out a single 64x64 array.

15

The four 32x32 images can thus be averaged digitally in the associated electronics, providing another factor of 2 in terms of improved noise performance. This takes the sensitivity down to 25mK and maintains the original frame rate. Reconfiguring the focal plane minimises the signal/image processing overhead, and enables frame rate to be maintained. Alternatively, the 32x32 array has a potential 50mK performance at 120Hz frame rate which may allow improved head tracking speed.

20

If the frame rate were then reduced by a factor of 4, a further improvement of a factor of two would be obtained, providing a 12.5mK sensitivity at 7.5Hz in this example. This would be very useful in an airbag head-position sensing application.

25

The above quoted improvements are dependent on careful design of the signal processing electronics and represent the best improvement obtainable.

- 5 -

One form of the invention will now be described, by way of example only, with reference to the accompanying drawings in which: -

Figure 1 is a schematic plan view of an array of detectors with associated circuitry;

5

Figure 2 is a sectional view of part of Figure 1;

Figure 3 is a schematic diagram showing connections to each detector for a conventional array; and

10

Figure 4 is a schematic diagram showing reconfigurable connections to each detector according to a first embodiment of the present invention.

Figure 5 is a thermal image of a driver in an automobile taken with a 64x64 array of detectors.

15

Figure 6 is a thermal image of a driver in an automobile taken with a 32x32 array of detectors.

20 Figure 7 is an algorithm showing the steps taken in processing the output of a detector array.

Figure 8 is a schematic diagram showing reconfigurable connections to each detector according to another embodiment of the present invention.

25

- 6 -

One detector array to which the present invention may be applied is shown in Figures 1 and 2. A thermal imaging array 1 comprises a base plate 2 of silicon onto which circuitry 3 such as amplifiers gates etc are grown. Preferably circuitry 3 includes the components to perform the process listed in the algorithm of Figure 7.

5 The array 1 has 4096 detectors arranged in a 64 x 64 array. Each detector 4 has associated therewith two row electrodes 5, 6 and a column electrode 7 for applying voltages to and reading output from each detector 4. All row electrodes 5, 6 are operated through a row driver 8, and all column electrodes 7 are operated through a column driver 9. Both drivers are controlled by a control circuit 10, which

10 communicates to external circuitry not shown.

Each detector 4 may be made as described in WO/GB00/03243. In such a device a micro bolometer 14 is formed as a micro-bridge 15 in which a layer of e.g. titanium is spaced about 1 to 4 μ m, typically 2.5 μ m, from a substrate surface 16 by thin legs 17,

15 18. Typically the titanium is about 0.1 to 0.25 μ m thick in a range of 0.05 to 0.3 μ m with a sheet resistance of about 3.3 Ω /sq in a range of 1.5 to 6 Ω /sq. The titanium detector microbridge 15 is supported under a layer 19 of silicon oxide having a thickness of about $\lambda/4$ where λ is the wavelength of radiation to be detected. Such a titanium detector can be adapted to detect a variety of wavelengths which include

20 those in the infra red radiation band between 8 and 14 μ m. The infrared energy is absorbed by the combination of layers 15 and 19, and the subsequent change in temperature causes the resistance of the titanium to change. Hence measuring the detector resistance provides a value of the incident radiation amplitude.

25 The detectors are all contained within an airtight container with walls 20 and a lid 21 forming a window or a lens. The walls 20 may be of silicon oxide and the window 21 of germanium, silicon, or a chalcogenide glass. Typically the pressure inside the container is less than 10Pa.

- 7 -

Figure 3 shows a typical conventional read out circuit. The array of resistors R_a , R_b , ... represent pixels in the array whose resistance value changes with temperature, and hence form a thermal detector array onto which radiation can be directed.

- 5 The resistor array is biased by a voltage ($+V_{bias}$). Each detector can be read out sequentially by switching on S_1 to activate the top row, and sequentially switching on S_a , S_b for the required integration time.

- 10 A balancing resistor R_{ref} of equal nominal value to the array resistors is connected to a negative bias voltage ($-V_{bias}$) which is equal in magnitude to $+V_{bias}$.

- 15 If the array resistor, e.g. R_a , and R_{ref} are at the same temperature, then no current is available to charge the integrating capacitor and the signal is zero. Any difference in resistance, however, is integrated over a chosen time period and represents, ideally, the temperature difference between an array resistor and the reference resistor.

- 20 The array resistors have a fixed thermal time constant which is a function of their thermal capacitance and thermal conductance. The operational amplifier will be optimised for a given input impedance, bandwidth and dynamic range.

- Figure 4 shows how each detector may be readout individually as a 64×64 array and connected together in groups of four to be read out as a 32×32 array. Two lines are shown with three detectors in each. A first line of detectors is indicated by resistances R_{1-1} to R_{1-64} each connected at one end to a $+V$ bias electrode 31 via a switch S_4 . The other ends of the resistances are connectable through switches S_{1-1} – S_{1-64} to a readout electrode connected through a switch S_1 to one end of a reference resistance R_1 and to an integrating capacitor amplifier 35. The reference resistance R_1 is connected to a negative bias voltage of equal amplitude to the $+V$ bias.

- 8 -

Similarly, the second line of detectors has resistances R_{2-1} to R_{2-64} connected via switch S5 to the +V bias, and via switches S_{2-1} to S_{2-64} , and S2 to an integrating capacitor amplifier 34, and reference resistance R2. Further switches S3 and S5 allow different combinations of connections as described below.

5

A relatively high definition thermal image is achieved by allowing each detector 4 to be illuminated by the scene through the window or lens 21 and reading each detector 4 separately. This thermal radiation alters the temperature of each detector and hence varying its resistance value. Each detector in the first line is then connected in turn, via switches S_{1-1} – S_{1-64} , to the amplifier 35 for an integration time. The amplifier 34 output voltage is thus proportional to the temperature of each detector. Similarly all other lines are read out. The collective output of all 64x64 detectors gives an electrical picture of the thermal scene to a good standard of detail. An example of such a 64x64 array is shown in Figure 5.

15

In order to change the focal plane array to effectively contain a quarter of the number of pixels, four array resistors can be connected in a serial/parallel fashion by introducing additional switches S3 and S5 as shown in Figure 4.

20

If S1 and S5 are kept open circuit and S2, S3, and S4 are closed, then the array can be scanned by closing groups of four pixel level switches at once – i.e., close S_{1-1} , S_{1-2} , S_{2-1} and S_{2-2} to read a “super pixel” composed of the four resistors R_{1-1} , R_{1-2} , R_{2-1} and R_{2-2} , whose combined resistance is nominally equal to R_{ref} , and whose thermal time constant is unchanged.

25

The result is reduced noise in the “super pixel” by a factor of 2 (noise improved by square root of 4), and an increased frame-rate by a factor of 4 (as there are only a quarter of the number of pixels to read out at the same sampling rate).

- 9 -

In order to maintain the performance of the array using pulse bias method, it may be necessary to increase the bias voltages by a factor of 2 to achieve a similar current flow through the each element. This may require the row amplifier to have sufficient dynamic range.

5

S3 introduces a small but additional resistance in the "superpixel" and this could be corrected for by adjusting the bias voltages accordingly, for example, increasing +Vbias slightly, or by introducing a matching switch in series with Rref.

- 10 The result of connecting detector pixels into groups of four is a 32x32 array; one example of this is shown in Figure 6. Comparing it with the 64x64 array of Figure 5, loss of definition is clear. Higher definition is useful in locating a head position, with the lower definition but faster readout image used for quick calculation e.g. in an accident.

15

Figures 8a-d show another arrangement for connecting detector pixels into groups. A 64 by 64 line and column array of pixels contains a first line of detector resistors R_{1-1} to R_{1-64} with successive further rows down to a sixty fourth row R_{64-1} to R_{64-64} , although only a four column by three row section is shown. A bias voltage line Vbias connect

20 to each column of resistors through switches a_1 to a_{64} . Output from each resistor to a column output line is through a switch marked c_{1-1} to c_{64-64} . Output from each column is via a switch d_1 to d_{64} . Switches b_1 to b_{63} connect the output line of one column to the bias line of its neighbour.

- 25 To operate at maximum resolution output is taken from each resistor R individually as shown in Figure 8b. All switches a_1 to a_{64} and d_1 to d_{64} are closed. Each line is read out successively a line at a time by closing all c switches in a line until all lines have been read.

- 10 -

To operate at 1/4th resolution, the resistors are connected together in groups of 4 in a serial and parallel arrangement so that their combined impedance is about that of a single resistor. This is shown in Figure 8c where resistors R_{1-1} , R_{1-2} , R_{2-1} and R_{2-2} are connected together closing switches a_1 , b_1 , c_{1-1} , c_{1-2} , c_{2-1} , c_{2-2} , d_2 ; the remaining
 5 resistors are similarly connected together.

To operate at 1/9th resolution, the resistors are connected together in groups of 9 in a serial and parallel arrangement so that their combined impedance is about that of a single resistor. This is shown in Figure 8d where resistors R_{1-1} , to R_{1-3} , R_{2-1} to R_{2-3} , R_{3-1} , to R_{3-3} are connected together closing switches a_1 , b_1 , b_2 , c_{1-1} , to c_{1-3} , c_{2-1} , to c_{2-3} , c_{3-1} to c_{3-3} d_3 ; the remaining resistors are similarly connected together in groups of 6.
 10

In a similar manner, the resistors may be connected together in groups of 4 by 4, 8 by 8, 16 by 16, and 32 by 32; which each group having the same nominal impedance as
 15 a single resistor. The resistors may also be arranged in groups of e.g. 5 by 5 or 6 by 6 etc. but this results in some pixels not being used, as is the case with the 3 by 3 array of Figure 8d where only 63 resistors in each line are used.

In the different arrangements shown, the resistors are grouped with adjacent resistors
 20 connected together. It is also possible to form groups but without connecting adjacent resistors. For example a 4 element group could be formed by connecting together resistors R_{1-1} , R_{1-3} , R_{3-1} , R_{3-3} with other resistors connected together in a similar manner and the complete array read out. Such an arrangement could interleaf, with a different grouping of 4 elements. For example groups formed by R_{1-2} ,
 25 R_{1-4} , R_{3-2} , R_{3-4} , and/or formed by R_{2-1} , R_{2-3} , R_{4-1} , R_{4-3} etc.

- 11 -

To increase sensitivity using off-chip techniques, digital image processing could be used to digitally average groups of four pixels. This would improve the noise by a factor of 2 but would not increase the frame rate. The present invention provides in addition to this improved noise value a faster frame rate (if required), or using digital averaging of the 4 frames obtained a further improvement of a factor of 2 in signal to noise. Off chip temporal averaging of frames means that the increase in effective time constant creates blurring in the image which is undesirable.

The technique of the present invention is twice as good in terms of noise, and permits the option of a four-fold increase in frame rate over the competing off-chip digital techniques. These are very useful advantages that allow lens system costs to be reduced and rapid information gathered when needed for fast moving events.

An example of the steps useful in processing the output of the detector array is shown in Figure 7.

Claims.

1. A reconfigurable detector array comprising:
a substrate (2) carrying an x by y array of detectors (4, 14, 15) each detector forming
5 a pixel, electrodes (5, 6, 7) for receiving an electrical signal from each detector
independently,
characterised by connections (S, a, b, c, d) for connecting separate detectors to be
read individually and into larger groups as required without changing substantially the
effective impedance.
10
2. The array of claim 1 wherein the detectors are resistance bolometers
3. The array of claim 1 wherein the array is an array of thermal detectors sensitive
within the range 3-14 μ m.
15
4. The array of claim 1 wherein the value of at least one of x and y lies in the range
24 to 96 inclusive.
5. The array of claim 1 wherein the substrate carries electronic circuitry for
20 processing the outputs of each detector and for reconfiguring the array into groups of
detectors.
6. The array of claim 1 wherein the detectors may be connected together in groups of
four adjacent detectors giving a 2x2 arrangement.
25
7. The array of claim 1 wherein the detectors may be connected together in groups of
sixteen adjacent detectors giving a 4x4 arrangement.
8. The array of claim 1 and including means for directing a scene onto the array.
30
9. The array of claim 1 wherein the array and substrate are encapsulated in a single
module with the detectors isolated from ambient conditions.

Fig.1.

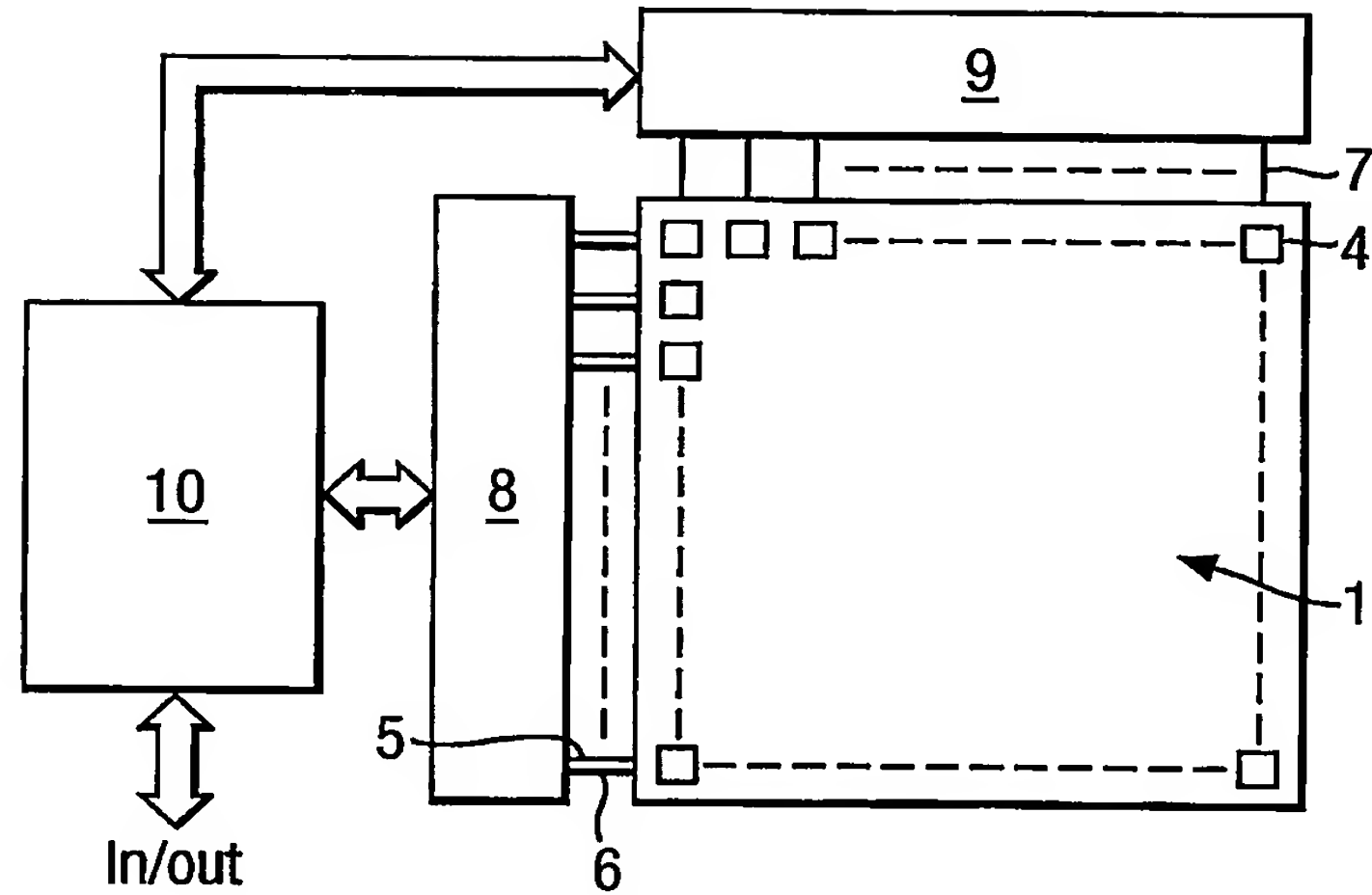


Fig.2.

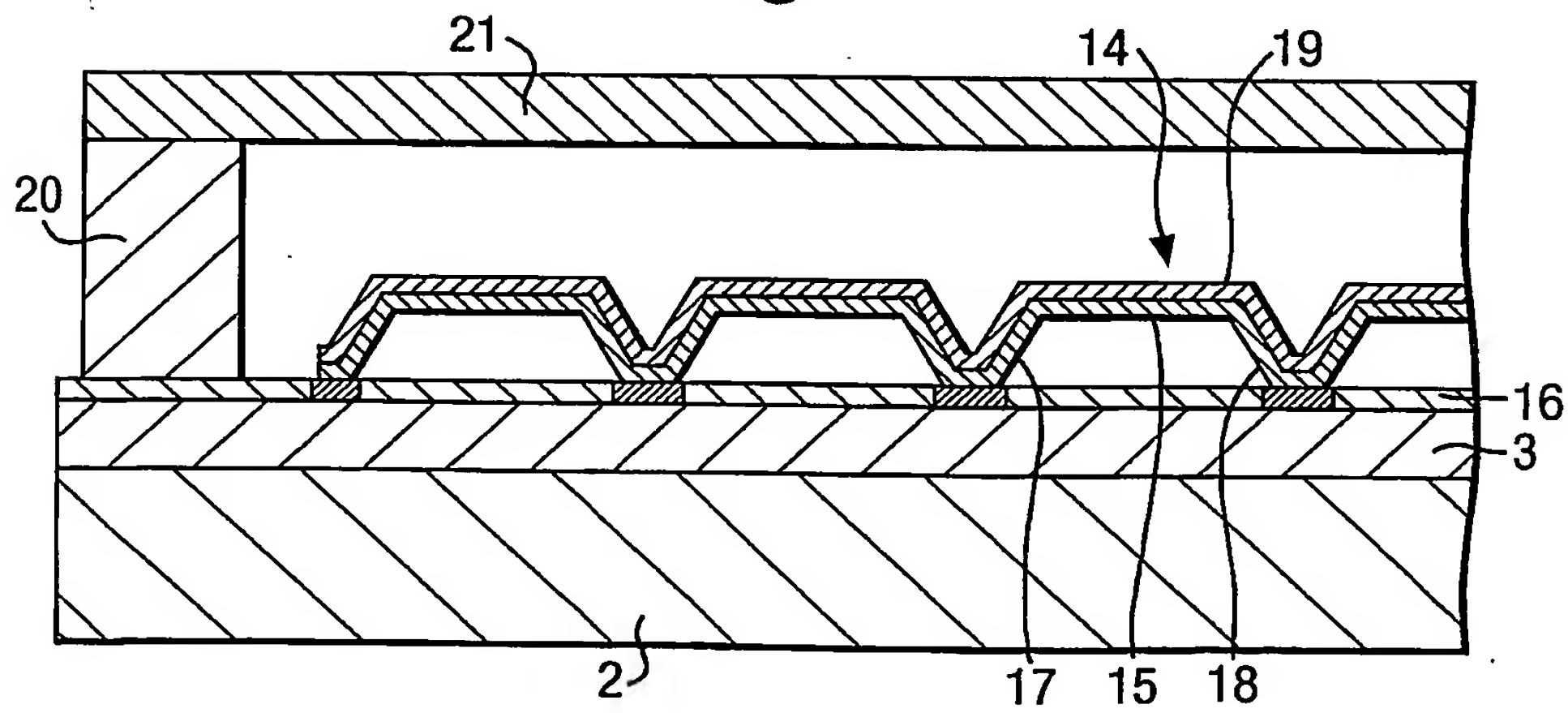


Fig.3.

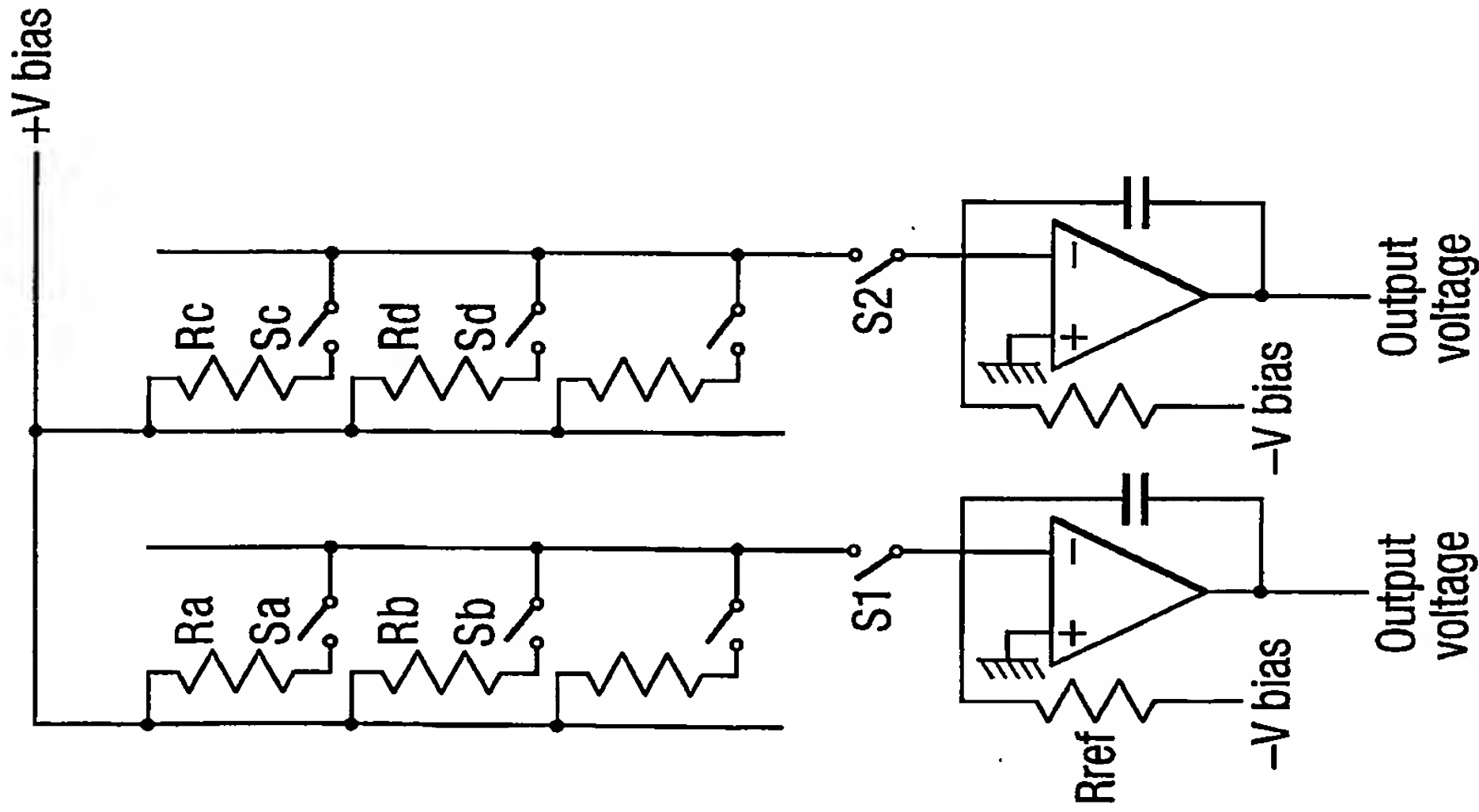
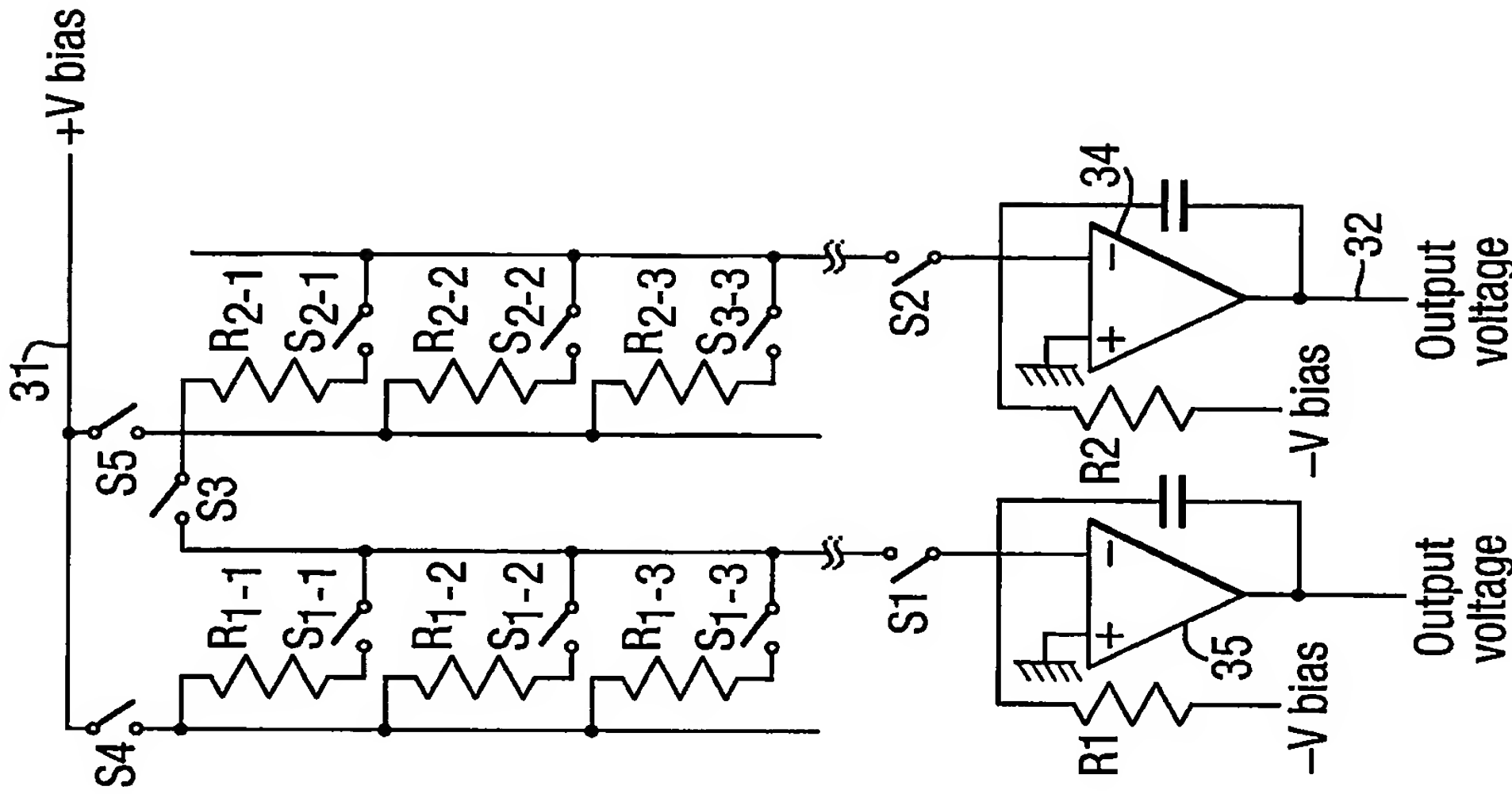


Fig.4.



3/5

Fig.5.

64x64 pixels



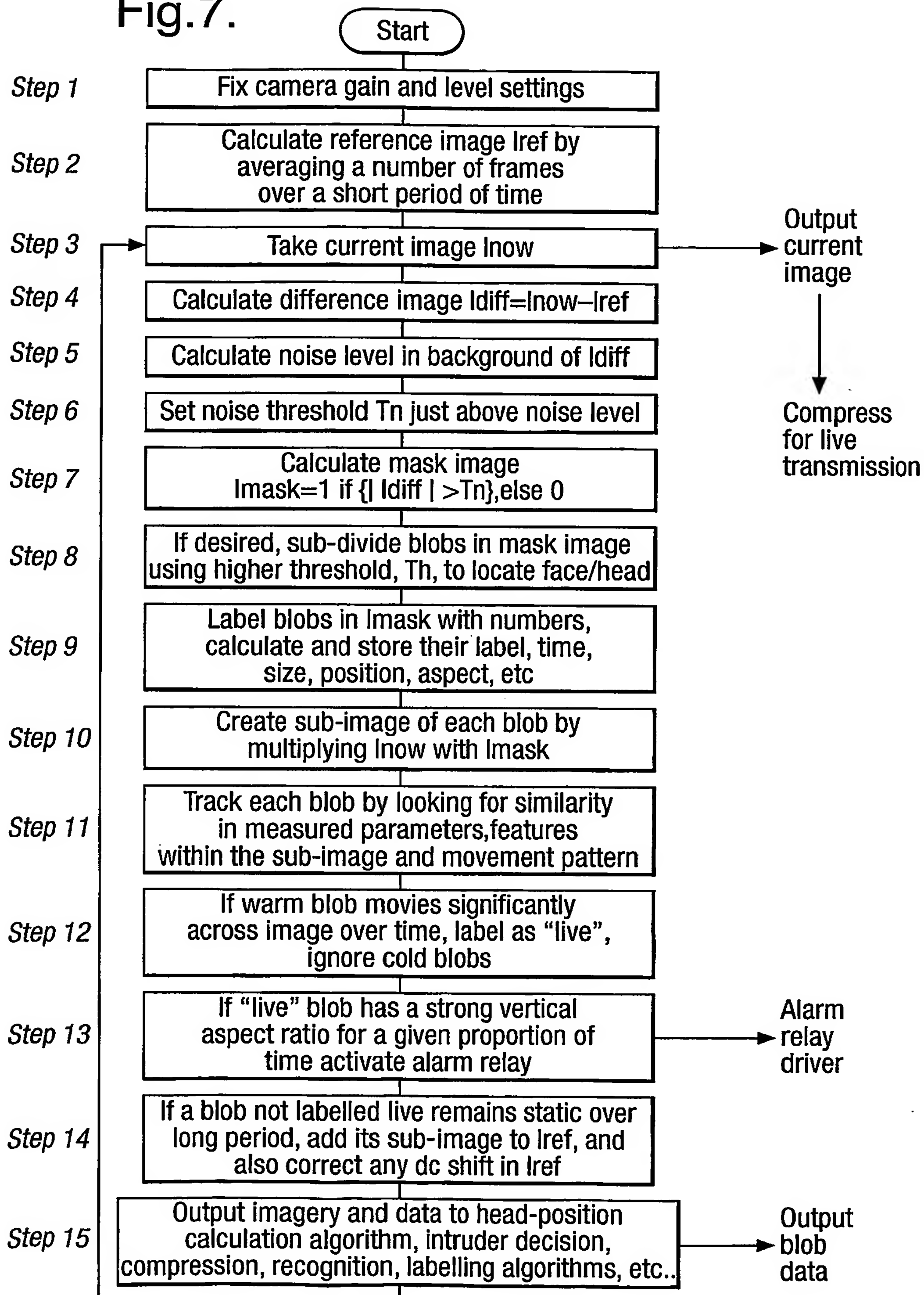
Fig.6.

32x32 pixels

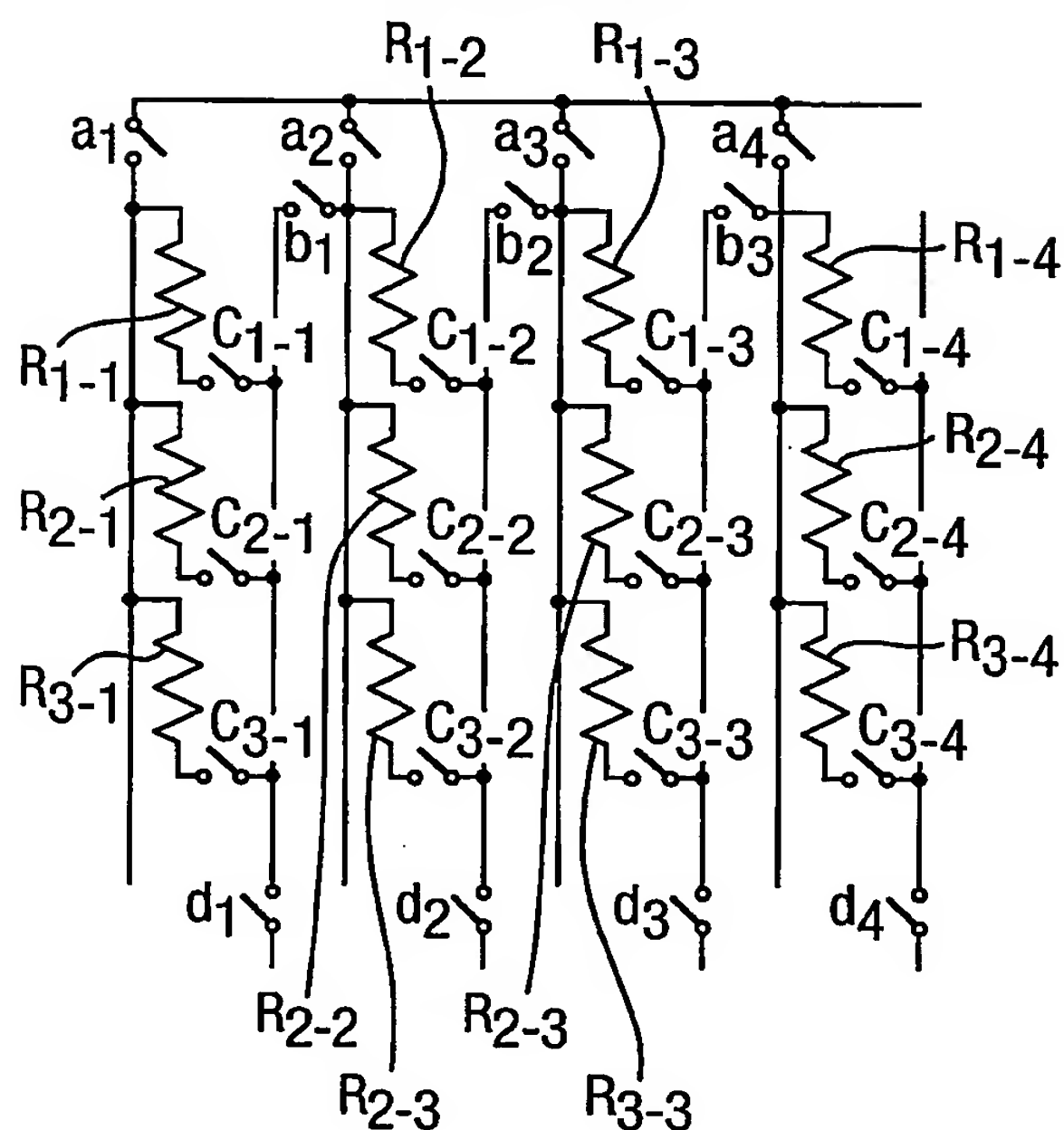
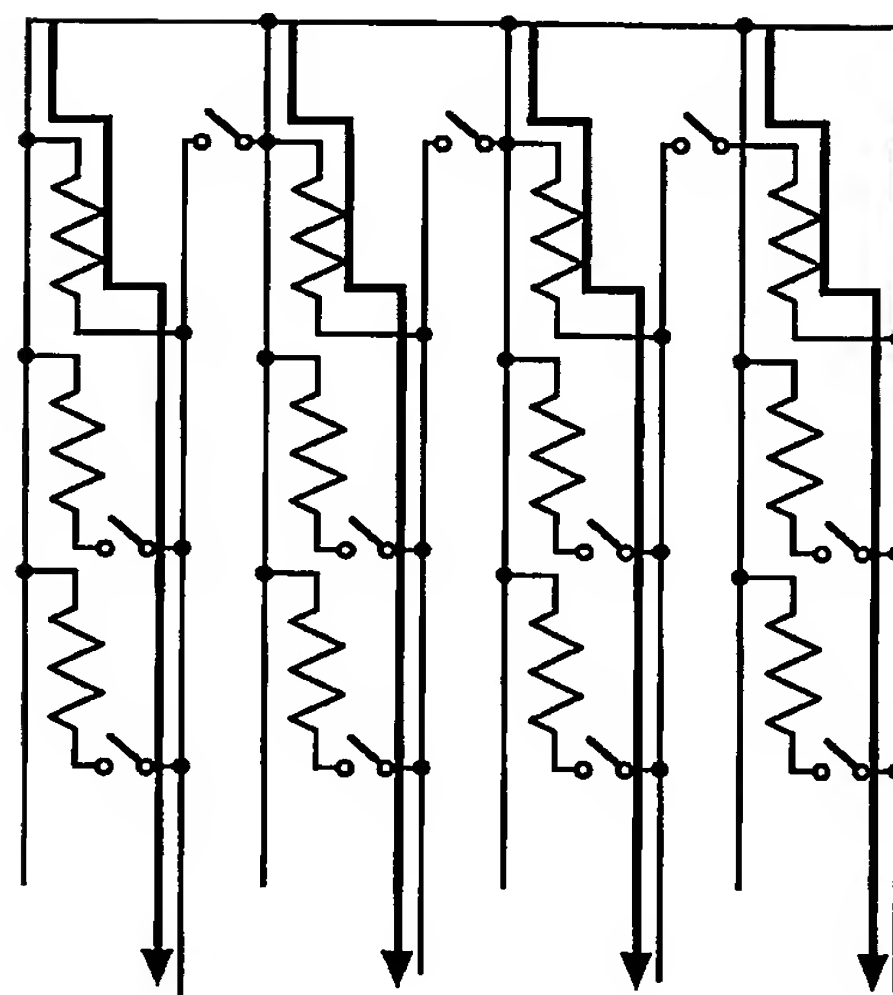
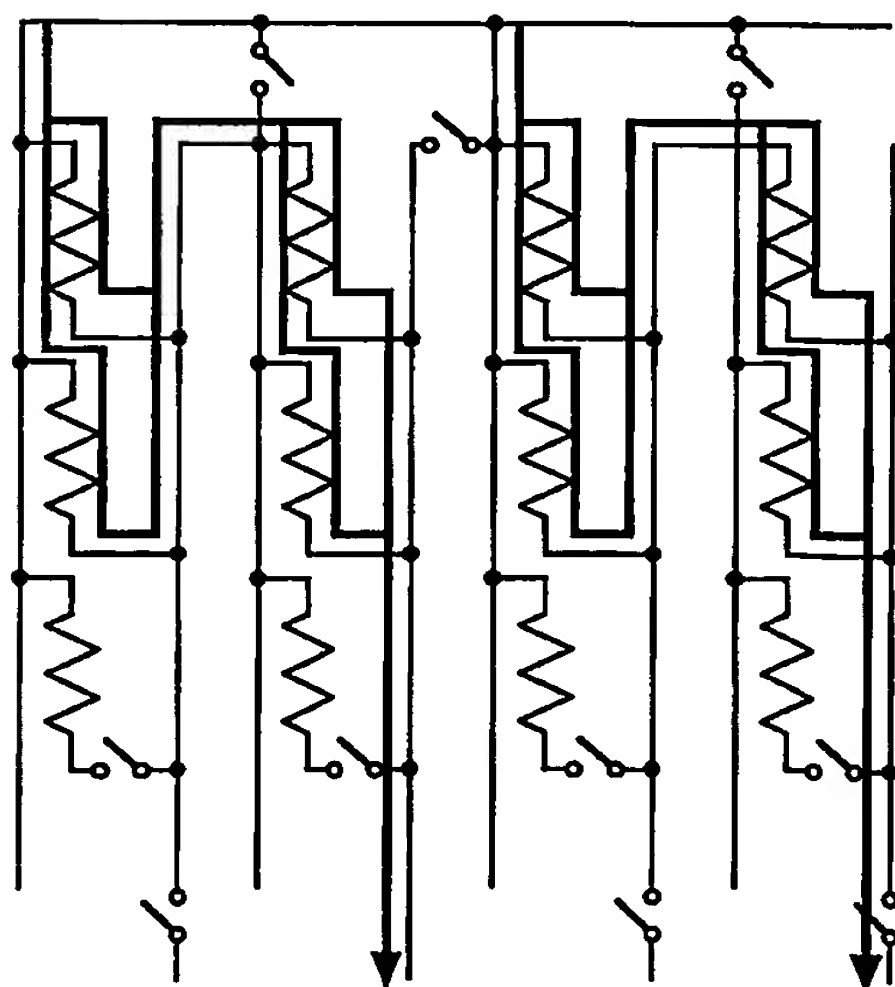
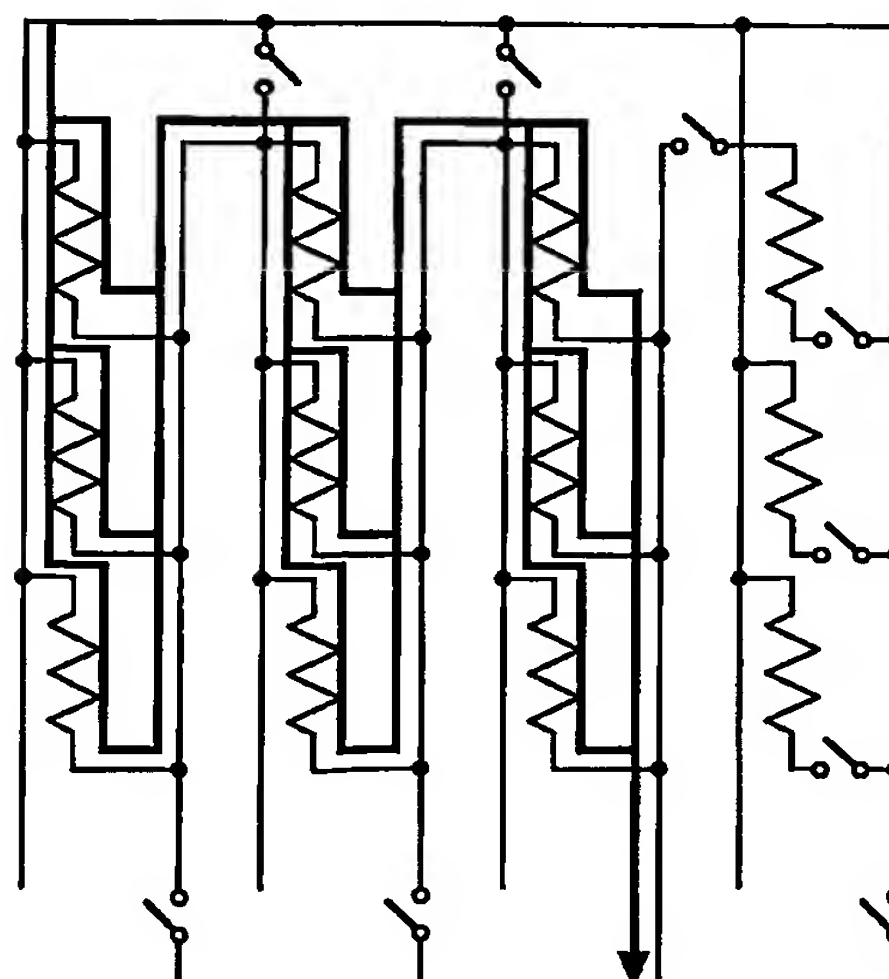


4/5

Fig.7.



5/5

Fig.8a.Arrangement of Pixels
and Switches**Fig.8b.**Arrangement for operation
at full resolution**Fig.8c.**Arrangement for operation
at 1/4 resolution**Fig.8d.**Arrangement for operation
at 1/9 resolution

INTERNATIONAL SEARCH REPORT

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 A. CLASSIFICATION OF SUBJECT MATTER
 IPC 7 H04N3/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

 Minimum documentation searched (classification system followed by classification symbols)
 IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

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☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

Application No
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